Electronic Version
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Claims

[c1] 1. A method of forming a low temperature polysilicon thin film transistor, comprising the steps of:
forming an amorphous silicon layer over a substrate;
performing a plasma treatment;
transforming the amorphous silicon layer into a polysilicon layer;
patterning the polysilicon layer to form a plurality of island polysilicon layers;
forming a channel region and a doped source/drain region on each side of the channel region in each island polysilicon layer; and
forming a gate over each channel region.

[c2] 2. The method of claim 1, wherein the step of performing the plasma treatment comprises applying an oxygen-containing plasma to adjust the threshold voltage in the negative direction.

[c3] 3. The method of claim 2, wherein the oxygen-containing plasma comprises nitrous oxide (N_2O) plasma.

[c4] 4. The method of claim 1, wherein the step of performing the plasma treatment comprises applying a hydro-

gen-containing plasma to adjust the threshold voltage in the positive direction.

[c5] 5. The method of claim 4, wherein the hydrogen-containing plasma comprises ammonia (NH_3) plasma.

[c6] 6. The method of claim 4, wherein the hydrogen-containing plasma comprises hydrogen (H_2) plasma.

[c7] 7. The method of claim 1, wherein the desired shift in the threshold voltage is effected by varying the radio frequency power to the plasma treatment.

[c8] 8. The method of claim 1, wherein the desired shift in the threshold voltage is effected by varying the processing period of the plasma treatment.

[c9] 9. The method of claim 1, wherein the step of patterning the polysilicon layer further comprises forming a gate insulation layer over the island polysilicon layers.

[c10] 10. A method of forming a low temperature polysilicon thin film transistor, comprising the steps of:
providing a substrate;
forming an amorphous silicon layer over the substrate;
performing a plasma treatment;
performing a laser annealing process to transform the amorphous silicon layer into a polysilicon layer;

patterning the polysilicon layer to form a plurality of island polysilicon layers;
forming a gate insulation layer over the island polysilicon layers;
forming a channel region in each island polysilicon layer and a doped source/drain region on each side to the channel regions; and
forming a gate over the channel regions.

[c11] 11. The method of claim 10, wherein the step of performing the plasma treatment comprises applying an oxygen-containing plasma to adjust the threshold voltage in the negative direction.

[c12] 12. The method of claim 11, wherein the oxygen-containing plasma comprises nitrous oxide (N_2O) plasma.

[c13] 13. The method of claim 10, wherein the step of performing the plasma treatment comprises applying a hydrogen-containing plasma to adjust the threshold voltage in the positive direction.

[c14] 14. The method of claim 13, wherein the hydrogen-containing plasma comprises ammonia (NH_3) plasma.

[c15] 15. The method of claim 13, wherein the hydrogen-containing plasma comprises hydrogen (H_2) plasma.

[c16] 16. The method of claim 10, wherein the desired shift in the threshold voltage is effected by varying the radio frequency power to the plasma treatment.

[c17] 17. The method of claim 10, wherein the desired shift in the threshold voltage is effected by varying the processing period of the plasma treatment.

[c18] 18. The method of claim 10, wherein the laser annealing process comprises performing an excimer laser annealing process.

[c19] 19. The method of claim 10, wherein the step of forming the amorphous silicon layer over the substrate, further comprises:
forming a silicon nitride layer over the substrate; and
forming a silicon oxide layer over the silicon nitride layer.

[c20] 20. The method of claim 10, wherein the step of forming a channel layer in each island polysilicon layer and a doped source/drain region on each side to the channel region further comprises:
forming a first patterned photoresist layer over the gate insulation layer to expose the upper surface of on each side of each island polysilicon layer; and
performing a p^+ doping process.

[c21] 21. The method of claim 20, wherein the step of performing the p^+ doping process further comprises removing the first patterned photoresist layer.

[c22] 22. The method of claim 10, wherein the step of forming a channel region in each island polysilicon layer and a doped source/drain region on each side to the channel region further comprises:
forming a second patterned photoresist layer over the substrate to cover a portion of the various island polysilicon layers and expose the upper surface on each side of the island polysilicon layers; and
performing an n^+ doping process.

[c23] 23. The method of claim 22, wherein the step of performing the n^+ doping process further comprises removing the second patterned photoresist layer.

[c24] 24. The method of claim 23, wherein the step of removing the second patterned photoresist layer further comprises:
forming a third patterned photoresist layer over the gate insulation layer to expose an area adjacent to the doped source/drain region of various island polysilicon layer; and
performing an n^- doping process to form lightly doped

drain regions.

[c25] 25. The method of claim 24, wherein the step of performing the n^- doping process further comprises removing the third patterned photoresist layer.

[c26] 26. The method of claim 10, wherein the step of forming a gate over the channel regions further comprises performing an activation process.

[c27] 27. The method of claim 10, wherein the step of forming a gate over the channel regions further comprises:
forming an inter-layer dielectric over the substrate;
forming a plurality of first openings in the inter-layer dielectric and the gate insulation layer to expose the doped source/drain regions; and
forming a plurality of source/drain metallic contacts over the inter-layer dielectric so that the source/drain metallic contacts and various doped source/drain regions are electrically connected via the first openings.

[c28] 28. The method of claim 27, wherein the step of forming a plurality of source/drain metallic contacts further comprises:
forming a passivation layer over the substrate;
forming a second opening in the passivation layer to expose a portion of the source/drain metallic contact; and

forming a pixel electrode over the passivation layer such that the pixel electrode and a portion of the source/drain metallic contact are electrically connected through the second opening.

[c29] 29. A low temperature polysilicon thin film transistor, comprising a polysilicon layer, a gate and a gate insulation layer, wherein the gate insulation layer is positioned between the gate and the polysilicon layer, the polysilicon layer has a channel region, and the concentration of oxygen within the channel region is between 1E19 to 1E23 atoms/cc while the concentration of hydrogen within the channel region is between 5E16 to 1E19 atoms/cc.

[c30] 30. The low temperature polysilicon thin film transistor of claim 29, wherein the transistor further comprises a plurality of doped source/drain regions positioned in the polysilicon layer on each side to the channel region.

[c31] 31. The low temperature polysilicon thin film transistor of claim 30, wherein the doped source/drain regions comprise p-doped regions.

[c32] 32. The low temperature polysilicon thin film transistor of claim 30, wherein the doped source/drain regions comprise n-doped regions.

[c33] 33. The low temperature polysilicon thin film transistor of claim 32, wherein the transistor further comprises a lightly doped drain region positioned between the doped source/drain region and the channel region.

[c34] 34. The low temperature polysilicon thin film transistor of claim 30, wherein the transistor further comprises an inter-layer dielectric positioned over the gate insulation layer with the inter-layer dielectric having a plurality of first openings that exposes the doped source/drain regions.

[c35] 35. The low temperature polysilicon thin film transistor of claim 34, wherein the transistor further comprises a plurality of source/drain metallic contacts for connecting electrically with the doped source/drain regions via the first openings.

[c36] 36. The low temperature polysilicon thin film transistor of claim 35, wherein the transistor further comprises a passivation layer positioned to cover the inter-layer dielectric and the source/drain metallic contacts such that the passivation layer has a second opening that exposes a portion of the source/drain metallic contact.

[c37] 37. The low temperature polysilicon thin film transistor of claim 36, wherein the passivation layer comprises a

silicon nitride layer.

[c38] 38. The low temperature polysilicon thin film transistor of claim 36, wherein the transistor further comprises a pixel electrode positioned over the passivation layer and electrically connected to a portion of the source/drain metallic contact via the second opening.

[c39] 39. The low temperature polysilicon thin film transistor of claim 38, wherein material constituting the pixel electrode comprises indium-tin oxide.